

# Survey of Architectures and Optimizations for Wide Bandwidth Envelope Amplifier

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**Abstract** — In the last years, RF power amplifiers are taking advantage of the switched dc-dc converters to use them in several architectures that may improve the efficiency of the amplifier, keeping a good linearity. The use of linearization techniques such as Envelope Elimination and Restoration (EER) and Envelope Tracking (ET) requires a very fast dc-dc power converter to provide variable voltage supply to the power amplifier but theoretically the efficiency can be much higher than using the classical amplifiers belonging to classes A, B or AB. The purpose of this paper is to analyze the state of the art of the power converters used as envelope amplifiers in this application. The power topologies will be explored and several important parameters such as efficiency, bandwidth will be discussed.

**Keywords** — Envelope Amplifier, Envelope tracking

## I. INTRODUCTION

In the past decades we have witnessed a tremendous growth of data transmission and as a direct consequence of this growth the need for highly spectrally efficient modulation has increased as well. One way to increase the amount of transferred data is to maintain the spectral efficiency constant and to increase the signal's bandwidth. Another is to use a more complex modulation and to increase the spectral efficiency for the given bandwidth. The trends regarding the signal's bandwidth and complexity can be seen in Figure 1 [1]. With modulations that are more complex it is necessary to apply phase and amplitude modulation at the same time, which directly leads to the use of power amplifiers that are able to provide linear amplification. Normally, from these PAs it is demanded to have wide bandwidth and high efficiency for very wide range of output power. The second condition is necessary due to very high Peak to Average Power Ratio (PAPR) of the transmitted signal. Linear PAs that belong to classes A, B or AB have high linearity, but suffer from very low efficiency with signals with high PAPR.

There have been several different concepts that have been used in order to obtain highly efficient wide-bandwidth linear amplification. One of these concepts is Doherty (proposed in 1936 [2]) which is based on modulation of the impedance and it is widely used in nowadays applications due to its simplicity [3]. Another concept is outphasing, originally proposed by Chireix in 1935 [4] to improve the efficiency of AM PAs. One implementation of this idea can be seen in [5].

In this paper the focus will be on another two techniques that have been widely exploited lately. The first is called Envelope Elimination and Restoration (EER), proposed by Kahn in 1952 [6]. The basic idea is shown in Figure 2. The RF signal, composed of simultaneous envelope and amplitude modulation, is decomposed in two paths. The phase modulation is amplified by highly efficient, yet nonlinear PA (classes E, D, F). On the other hand, the envelope modulation is injected through the modulation of the power supply. The block that performs this part is called Envelope Amplifier (EA), which is actually a wide bandwidth, high efficiency dc-dc converter that has to

follow envelope reference. Envelope Tracking (ET) is a similar concept, where instead of a non-linear PA (like in EER) a linear PA is used. The linear PA performs the complete modulation, while the EA just adjusts its output voltage as close as possible to the value of the RF envelope so the linear PA works in the area of high efficiency.

In order to obtain a highly efficient EA the solutions based on a switching dc-dc converter normally are employed. However, in some applications the desired bandwidth is very high, so that a switching dc-dc converter with high switching frequency (usually 7-10 times higher than the desired bandwidth) is not sufficiently efficient. Therefore, some hybrid solutions based on a combination of a linear regulator and a switching dc-dc converter are used. In the following paragraphs different architectures for EA that can be found in the state will be presented. The solutions vary depending on the needed bandwidth (from hundreds of kHz to tens of MHz) and the output power range (from few W to several kW). An optimization method for each of these architectures will be presented and explained.

## II. CLASSIFICATION OF THE SOLUTIONS FOR EA

One possible way how to systematize the solutions is presented in Table I. There can be distinguished five different architectures and Figure 3 shows simplified schematics of possible architectures. In this figure, most of the diodes are implemented with controlled switches (MOSFETs due to the high switching frequency) but we keep the diodes for the sake of clarity of the circuits.

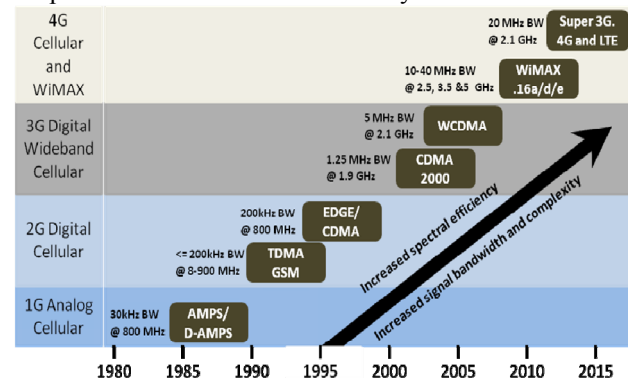


Fig.1. Evolution and trends in wireless standards

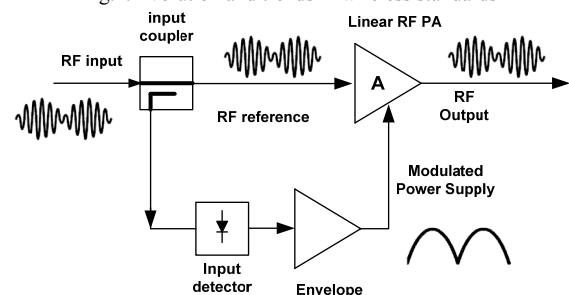


Fig.2. Simplified block schematic of Envelope Elimination and Restoration concept

#### A. Single input single output converter

As it has been said before, a switching dc-dc converter offers high efficiency and in the state of the art there can be found many solutions based on a buck converter due to its simplicity. Buck converter is a very attractive solution when it is necessary to implement a solution for an integrated PA [7-9]. These solutions operate at extremely high switching frequencies (up to 200MHz) in order to minimize the size of passive components and facilitate the integration. The output power rarely exceeds few watts and the obtained bandwidth is in range of MHz.

However, for higher output power and lower bandwidths, it is possible to find a buck converter that is implemented with discrete components, like in the case of [10] where the output power is 500 W and desired bandwidth around 50 kHz.

In both cases, it is necessary to optimize the design of the output filter and the switching frequency in order to minimize the overall switching losses. [11, 12] or the size of the converter.

When it is necessary to obtain wide bandwidth of the envelope amplifier, it is very common to use a hybrid solution based on a buck converter in parallel with a linear regulator [13-16]. The idea is based on the fact that the major part of the envelope energy lies in the low frequency part of the spectrum, while the high frequency part, which defines the bandwidth of the EA, is practically negligible from the point of view of the envelope's energy. In this configuration the buck converter usually operates as a current source, while the linear regulator has to control the output voltage. However, it is possible to have both parts

operating as a voltage sources [14, 17], although it can complicate the design of the EA.

It has been shown that only the dc portion of the envelope has around 80% of the total envelope energy [18]. Therefore, it would be possible to make a highly efficient dc-dc buck converter that would produce just this part of the envelope while the linear regulator has to deal with the complete envelope's dynamics [13, 18]. In the major part of the solutions, the linear regulator is controlled with a hysteretic control that sets its dc current to zero. Nevertheless, in [13, 18] it has been shown that depending on the transmitted signal it is not necessarily the optimum solution from the point of EA's efficiency. A method that explains how to optimize the EA from the point of view of its efficiency and size has been presented in [18]. It has been shown that there is a relationship between the size and efficiency of the EA and that there exists the optimum dc current that has to be supplied by the buck converter in order to obtain the maximal efficiency. Figure 4 shows how the efficiency of the EA is changed depending on the value of the buck's dc current for different signals.

TABLE I

SYSTEMATIZATION OF THE STATE OF THE ART SOLUTIONS FOR THE EA

Group	Topology	Linear regulator
A	A.1 Buck converter	None
	A.2 Buck converter	Parallel
B	Multiphase converter	None
C	C.1 Multi input converter	None
	C.2 Multi input converter	Parallel
D	Multilevel converter	Series
E	Multiphase converter	Series

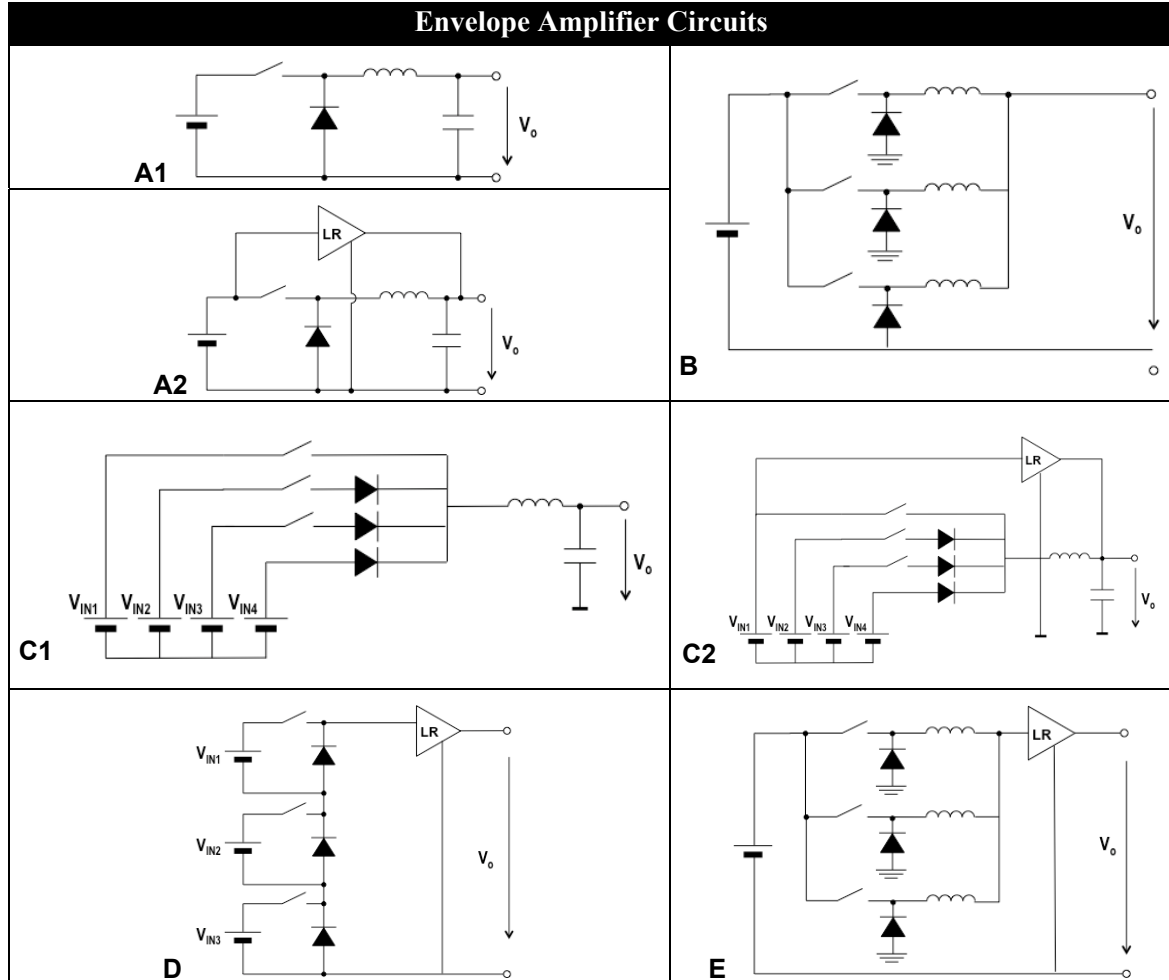


Fig.3. Simplified schematics of possible architectures for highly efficient wide bandwidth Envelope Amplifier

However, the buck converter can process more energy than just the dc portion of the envelope. By increasing the bandwidth of the buck converter, it will process more energy in an efficient way, but it is necessary to increase its switching frequency in order to process higher part of the envelope's spectrum. What can be expected is that the EA's efficiency is firstly going to increase (due to efficient buck converter), but beyond a certain bandwidth the power losses in the buck converter will be so high that the EA's efficiency starts to drop. In [17, 18] this optimization has been analyzed and it has been shown that the optimum bandwidth of the buck converter is very low. The main reason for this is that the switching losses of the buck converter increase faster than the amount of the energy processed by the buck converter. Figure 5 shows how the energy processed by the buck converter changes depending on its bandwidth. In the same figure it can be seen how the EA's efficiency is changed for different MOSFETs that are employed in the buck converter. By using new GaN transistors it could be possible to increase the overall efficiency for, approximately, 7%. This efficiency improvement should be taken with precaution, because in the efficiency estimation the power losses in the output filter have not been concerned and this part of the losses can be very high.

### B. Multiphase converter

In many applications instead of a single buck converter a multiphase converter is used. This type of converters allows to decouple the switching frequency of the output voltage ripple. The use of several shifted power stages (phases) can be a good solution due to their reduced output voltage ripple since usually this is one of the requirements for the envelope amplifiers. This solution has been used in [19] to track a 250W-11kHz envelope by means of a 4-phases buck converter with very high efficiency. Regarding the bandwidth, it can be higher than its switching frequency in the multiphase converters but it is far of being the switching frequency multiplied by the number of phases as shown in [20]

### C. Multiple-Input Buck Converter

In order to increase the bandwidth of the buck converter it is necessary to implement an output filter that would allow fast dynamics of the output voltage and current. In the case of a classical buck converter it leads to a solution that has a big current and voltage ripple, something that is not desirable in the case of EA. The inductor of the classical buck converter has one terminal that is connected to the output, while the second switches between the ground and the input voltage. If the inductor has low inductivity, it could lead to a very high current ripple. If the buck converter were supplied by a several voltages, the second terminal of the inductor would switch between two voltage levels that are significant lower than in the previous case. In that way, for the same value of the inductor and the output power the current ripple would be much lower and, consequently, the voltage ripple as well. This is the basic idea of a multiple input buck converter that can be seen in Figure 3.

Using this idea an EA with the bandwidth of 100 kHz and output power of 50W has been implemented in [21]. One of the advantages of this architecture is that the transistors that are used have to support significantly lower voltages than in the case of a classical single buck. In this way, they could be optimized in order to operate at high switching frequencies exhibiting very low switching losses.

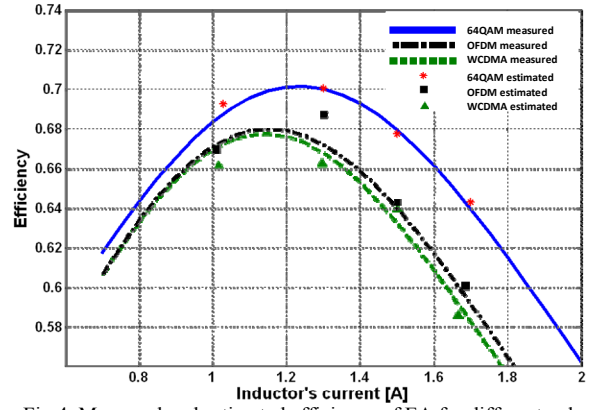


Fig. 4. Measured and estimated efficiency of EA for different values of the buck's dc current

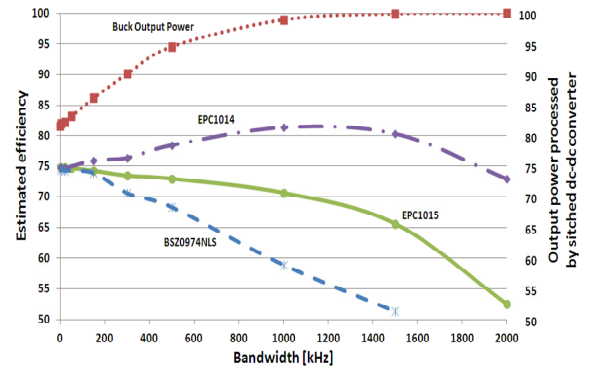


Fig. 5. Dependency of the energy processed by the buck converter and EA's efficiency depending on the bandwidth of the buck converter

Possible way how to optimize this architecture towards the maximum efficiency would be to determine the optimum number of the input voltages and its distribution. The equidistant voltage distribution is not necessarily the best having in mind that the envelope has Rayleigh's distribution and that some voltage levels have to provide more energy than the others do.

In figure 3 and in [21] the switches that are used are represented as a series combination of a transistor (MOSFET) and a diode that has to be placed in order to prevent a short circuit between the voltage supplies via the intrinsic MOSFET diode. However, the switch that is needed for this converter can be implemented using two MOSFETs in series with their sources connected. This would lead to lower conduction losses of the switching converter.

### D. Multiple-Input Buck Converter in parallel with a linear regulator

Like in the case of a classical buck converter, it is possible to use a linear regulator in parallel with a multiple input buck converter. The reason is the same as in the aforementioned architectures. In this way it is possible to implement a wide bandwidth EA using a switching converter with low switching frequency. In [22] this idea is presented and tested. However, in [22] the connection between the linear regulator and a switching converter has not been implemented as it is normally done, when the linear regulator operates as a voltage source and the buck converter as a current source. In [22] these two parts are connected via two antiparallel diodes. This implementation is very simple, and the linear regulator operates only when the slew rate of the envelope is higher than the slew rate of the buck's inductor. If the bandwidth of the buck converter is close to the bandwidth of the envelope, the linear regulator will not process huge amount of energy.

Nevertheless, if the bandwidth of the buck converter is not designed correctly it could lead to very poor efficiency because the linear regulator would process complete energy of the envelope.

Therefore, for this architecture it is clear that the main optimization parameters would be the bandwidth of the switching converter, which leads, once again, to the optimization of the number of the voltage supplies and their distribution.

#### E. Multilevel converter in series with a linear regulator

In order to exploit good characteristics of a linear regulator, an architecture that is composed of a multilevel converter in series with a linear regulator is proposed in [23]. Similar solution can be found in a commercially available EA [24]. The role of the switched converter is to make a first approximation of the envelope voltage from the input voltage in a low dissipative way. The input voltage is reduced dynamically according to the shape of the reference to reduce the power losses on the linear regulator (figure 6). The linear part will receive the same reference and it is the responsible of providing at its output the envelope required by the power amplifier.

In terms of efficiency this solution is better than a single linear regulator but it is necessary to obtain quite high efficiency in the switched part. The switched regulator can be implemented in many different ways [25, 26] (Figure 3 shows just one possible way how to do it). The multilevel converter operates in open-loop and its output will be only certain discrete voltage levels. These levels are achieved by stacking cells (see figure 3) or by an analog multiplexor [26]. The main advantage is that the average switching frequency of these cells is much smaller than the frequency of the envelope (it depends on the probability density of the envelope), obtaining a high efficiency. In [18] it is explained how the average switching frequency could be estimated for a signal described by its probability function. Figure 7 shows a comparison between the estimation and a real switching frequency in the case when the envelope of a 2MHz 64QAM signal is processed.

The presence of the linear regulator makes unnecessary the output filter. These circuits have been used for an EER amplifier and this envelope amplifier provides 100W peak power with 2MHz bandwidth [27]. Moreover, they also may work well in an ET configuration by removing the linear regulator.

Similar to the architecture C, the number of the voltage levels and their distribution can be optimized. Figure 8 shows the EA's efficiency for different numbers of voltage levels and comparison between the optimal and equidistant distribution of the levels.

It is interesting to compare this solution, where the linear regulator is in series, and the solution A.2 where the linear regulator is in parallel [18]. In the series configuration to improve the efficiency a higher number of levels is required while in the parallel the efficiency is improved if the bandwidth of the switched part is improved. In both cases there is a trade-off since the increment of the number of levels very much penalizes the efficiency and improving the bandwidth forces to increase the switching frequency. In general terms, it can be said that the series approach may provide a better efficiency (around 10%) by means of a higher complexity.

In three last categories (C1, C2 and D), it is the role of the designer to generate the auxiliary voltage levels from the available source. In general, there is only one voltage supply available and a multi-output converter should be

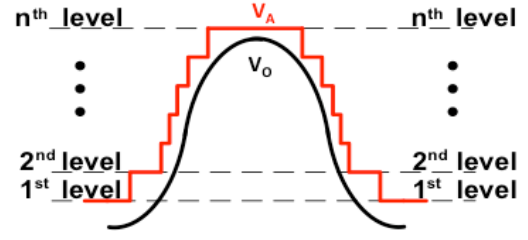


Fig. 6. Voltage waveform at the input of the linear rectifier and output voltage using the multilevel converter in series with a linear regulator

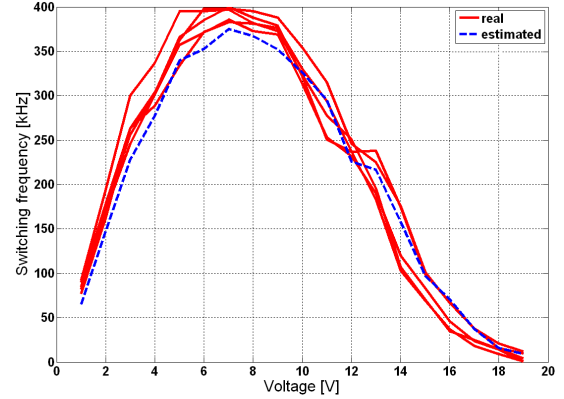


Fig. 7. Comparison of the real and estimated switching frequency for the multilevel converter depending on the level of transition

included as a first stage to generated these voltage levels. The topology for this first stage may vary depending on the particular values of the voltages and we should consider the cross regulation of the outputs. The advantage is that since it does not have any dynamic requirements it can be designed with a low switching frequency to avoid a big penalization of the efficiency. In [23] a flyback converter with three outputs has been used. In [25] a bidirectional flyback in a combination with a buck converter was implemented as a first stage, while in [26] the first stage is composed of simple voltage dividers implemented with switched capacitors. The last example offers very high efficiency and power density of the first stage and it does not need any bulky magnetic component, which opens a possibility for the integration of this stage.

#### F. Multiphase Converters plus Series Linear Regulator

As it is very well known in a multiphase converter with  $N$  phases, duty cycles that are equal to  $i/N$  ( $i=[1..N]$ ) lead to total ripple cancelation. In theory it means that the output capacitor is not necessary. On the other hand, in practice, there is need for small capacitor due to small asymmetries of the phases and small current ripple that is present. Due to the small capacitance of the output filter, it

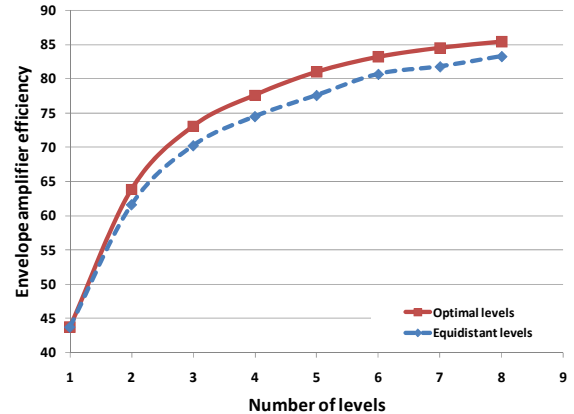


Fig. 8. Efficiency of the envelope amplifier when it is implemented with optimized and equidistant voltage levels



is possible to change the output voltage very fast. In [28, 29] this idea has been used in order to implement a multilevel converter. In both references the multiphase converter operates only with discrete duty cycles, having the multiphase converter operating in the so called “node” when the ripple cancelation is obtained. In [28] this multilevel converter is used for ET and it supplies a linear PA. Voltage changes are performed by changing the duty cycle between the needed values. On the other hand, in [29] the voltage changes are performed in the theoretically minimal time, using the Pontryagin’s minimum principle [30]. The minimum time transition is very well known technique for a single buck converter. In the case of a multiphase converter it is not easy to implement it. However, if the duty cycles that are used are always “node” duty cycles, it facilitates the implementation a lot, because in the steady state there is not any current through the output capacitor and it eases the calculus of the transition times as it has been shown in [29]. In [29] a 4 phase multiphase converter with minimum time transient is implemented and it can be used for ET or for EER (in combination with a linear regulator). Figure 9 shows gate voltages during the transient. It is important to notice that the transition time is equal for each phase. What is different is the ON and OFF duration of the gate pulse. The reason for this is different instantaneous currents in each phase due to the current ripple. Figure 10 shows one transient where it can be seen that the transition time is faster than one switching cycle and that the transition is smooth, without any overshoot. The phase currents are shown as well. By optimizing the design of the output filter of the multiphase converter together with the number of phases it is possible to optimize the transition speed. By increasing the number of the phases, the linear part of the system (both in ET and EER) will have higher efficiency, but the complexity will be much higher.

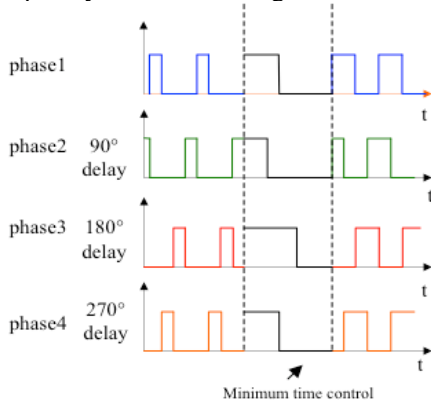


Fig. 9. Gate voltages of the multiphase converter working with discrete duty cycles applying minimum time technique in the transitions

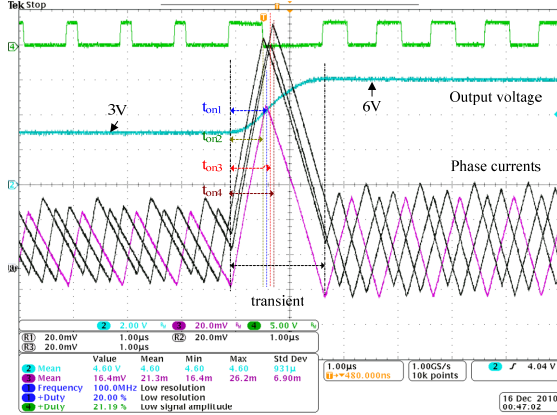


Fig. 10. Output voltage step from 3V to 6V,  $f_{sw}=1\text{MHz}$  (2V/div) and phase currents (200mA/div),  $L=6.8\mu\text{H}$ ,  $C=1\mu\text{F}$

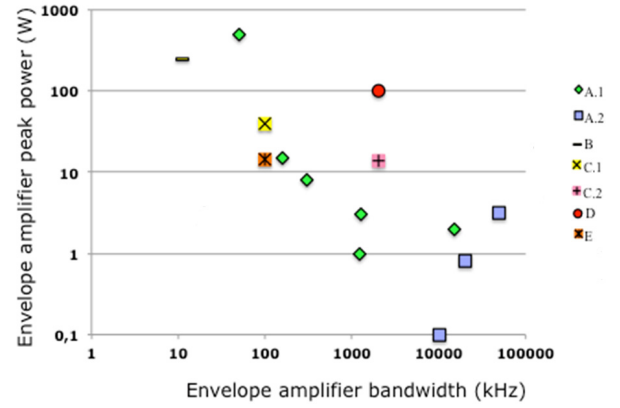


Fig. 11. Maximum bandwidth and peak power of the analyzed topologies for reference tracking

The problem of this solution is that if the transient should be very fast, the limited resolution of the digital control device may be a restriction to perform the minimum time transition with accuracy and the switching frequency is very similar like in the case of a classical multiphase buck converter controlled by PWM.

### III. TRADE-OFF BANDWIDTH-OUT TRADE-OFF BANDWIDTH-OUTPUT POWER

Figure 11 shows a comparison of the solutions presented in the state of the art according to the trade-off envelope bandwidth and output power (note the log scale in both axis). Classical topologies (group A1) cover both parts, wide bandwidth [7] and high power [10], but not simultaneously. Including a parallel linear regulator (group A.2) makes easier to achieve a high bandwidth [15, 16]. The solution that presents a good trade-off between power and bandwidth is the one based on the multilevel with series regulator [23-27]0 (group D).

The use of new devices with lower switching losses may help to increase the efficiency of the switched converters for envelope amplification in higher bandwidth application. In particular GaN technology is suitable for this purpose. Some research groups are now testing GaN devices from EPC for improving dc-dc converters [31, 32] and this application in particular [33]0. The first results seem promising but, of course, the technology is not mature and better results are expected in the next future.

### IV. CONCLUSIONS

Many papers have been reported where the use of switched converters in structures such as EER and ET, improve the efficiency of the RFPA in the range 5-20% compared with the classical amplifiers. The role of this converter is to provide the envelope voltage for the power amplifier. In most of the cases, the topology is a buck converter due to its high efficiency. However, when a high bandwidth is required, the switching frequency should be so high that the power losses limit the amount of power that these converters can provide. For medium power range other alternatives can be found. All of them use several switches and they are based on multiphase or multilevel converters. They are more complex but particular advantages can be obtained such as a reduced filter or a better efficiency. In many cases, the use of a linear regulator in parallel with the switched converter improves the bandwidth very much by means of efficiency penalization. The last option is to connect this linear regulator in series with the switched converter. This configuration allows the use of a power stage that may work at a reduced switching frequency because the voltage applied to the power

amplifier is shaped by the linear regulator. This solution shows a good trade-off between maximum power and bandwidth of the envelope.

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